Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended) A system for maintaining cache coherency in a CMP comprising:

one or more processor cores;

[[a]] an on-chip shared cache; and

a ring, wherein the ring ~~connects~~ to connect the one or more processors and the shared cache[[;]] .

Claim 2 (Original)The system of claim 1 wherein the one or more processor cores each include a private cache.

Claim 3 (Original)The system of claim 1 wherein shared cache includes one or more cache banks.

Claim 4 (Original)The system of claim 3 wherein the one or more cache banks is responsible for a subset of a physical address space of the system.

Claim 5 (Original)The system of claim 1 wherein the one or more processor cores are write-thru.

Claim 6 (Original)The system of claim 5 wherein the one or more processor cores writes data through to the shared cache.

Claim 7 (Original)The system of claim 1 wherein the one or more processor cores includes a merge buffer.

Claim 8 (Original)The system of claim 7 wherein data is stored in the merge buffer.

Claim 9 (Original) The system of claim 8 wherein the merger buffer purges data to the shared cache.

Claim 10 (Original) The system of claim 1 wherein the one or more processor cores accesses data from the shared cache.

Claim 11 (Original) The system of claim 8 wherein the merger buffer coalesces multiple stores to a same block.

Claim 12 (Original) The system of claim 1 wherein the ring is a synchronous, unbuffered bidirectional ring interconnect.

Claim 13 (Original) The system of claim 12 wherein a message has a fixed deterministic latency around the ring interconnect.